WHAT IS CLAIMED IS:

1. A semiconductor device interposed between an input/output terminal and a ground terminal of a semiconductor integrated circuit, and serving as a protecting element for protecting said semiconductor integrated circuit against electrostatic discharge, said semiconductor device comprising:

an emitter electrode provided on a first main surface of a semiconductor substrate;

a P-type base region disposed in a surface of said first main surface and containing P-type impurities;

an N-type emitter region selectively disposed in a surface of said P-type base region, containing N-type impurities at a relatively higher concentration, and contacting with said emitter electrode;

a base contact region selectively disposed in a surface of said P-type base region, spaced from said N-type emitter region with a spatial clearance, and containing P-type impurities at a relatively higher concentration;

a base electrode disposed on said base contact region; and

an N-type collector region disposed in a surface of said second main surface, containing N-type impurities at a relatively higher concentration, and electrically contacting with a collector electrode; wherein

said emitter electrode is connected to said input/output terminal; and

said base electrode and said collector electrode are connected to a ground potential.

2. The semiconductor device according to claim 1, further comprising a first

P-type impurity region formed in said P-type base region located beneath said N-type emitter region so as to contact with said N-type emitter region.

3. A semiconductor device interposed between an input/output terminal and a ground terminal of a semiconductor integrated circuit, and serving as a protecting element for protecting said semiconductor integrated circuit against electrostatic discharge, comprising:

first and second NPN transistors and a PNP transistor, wherein

said first and second NPN transistors have emitters being commonly connected, said first NPN transistor has a collector and a base connected to said input/output terminal, and said second NPN transistor has a collector and a base connected to said ground terminal, and

said PNP transistor has a base commonly connected to said emitters of said first and second NPN transistors, an emitter connected to said input/output terminal, and a collector connected to said ground terminal.

4. The semiconductor device according to claim 3, wherein

said semiconductor device comprises:

a low-concentration N-type impurity region disposed in a surface of a first main surface of a semiconductor substrate and containing N-type impurities at a relatively lower concentration;

an N-type emitter region selectively disposed in a surface of said low-concentration N-type impurity region and containing N-type impurities at a relatively higher concentration;

first and second P-type base regions selectively disposed in a surface of said

low-concentration N-type impurity region in such a manner that said N-type emitter region is located between said first and second P-type base regions and each of said first and second P-type base regions has a portion contacting with said N-type emitter region;

first and second N-type collector regions selectively disposed in respective surfaces of said first and second P-type base regions so as to be spaced from said N-type emitter region, and containing N-type impurities at a relatively higher concentration; and

first and second base-collector common electrodes respectively contacting with portions of said first and second N-type collector regions exposed at the same level with exposed surfaces of said first and second P-type base regions, and also contacting partly with said exposed surfaces of said first and second P-type base regions, wherein

said first base-collector common electrode is connected to said input/output terminal,

said second base-collector common electrode is connected to said ground terminal, and

said N-type emitter region corresponds to said emitters of said first and second NPN transistors and also corresponds to said base of said PNP transistor.

5. The semiconductor device according to claim 4, further comprising a plurality of P-type impurity regions selectively disposed in surfaces of portions in which both of said first and second P-type base regions contact with said N-type emitter region and form a P-N junction, respectively, and also selectively disposed in the surfaces of said first and second P-type base regions at portions corresponding to bottoms of said first and second N-type collector regions, and said P-type impurity regions containing P-type impurities at a lower concentration compared with said first and second P-type base regions.

6. The semiconductor device according to claim 4, further comprising a high-concentration N-type impurity region contacting with an entire surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate, and containing N-type impurities at a relatively higher concentration, wherein

said high-concentration N-type impurity region is connected to a ground potential.

7. The semiconductor device according to claim 4, further comprising a high-concentration N-type impurity region contacting with a surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate, and containing N-type impurities at a relatively higher concentration, wherein

said high-concentration N-type impurity region is maintained at a floating potential.

8. The semiconductor device according to claim 4, further comprising an insulating layer contacting with a surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate.

9. A semiconductor device interposed between an input/output terminal and a ground terminal of a semiconductor integrated circuit, and serving as a protecting element for protecting said semiconductor integrated circuit against electrostatic discharge, comprising:

an NPN transistor, a PNP transistor, and a diode, wherein

an emitter of said NPN transistor, a base of said PNP transistor, and a cathode of said diode are commonly connected,

an anode of said diode and an emitter of said PNP transistor are connected to said input/output terminal,

a collector and a base of said NPN transistor are connected to said ground terminal, and

a collector of said PNP transistor is connected to said ground terminal.

10. The semiconductor device according to claim 9, wherein

said semiconductor device comprises:

a low-concentration N-type impurity region disposed in a surface of a first main surface of a semiconductor substrate, and containing N-type impurities at a relatively lower concentration;

an N-type emitter region selectively disposed in a surface of said low-concentration N-type impurity region, and containing N-type impurities at a relatively higher concentration;

first and second P-type base regions selectively disposed in a surface of said low-concentration N-type impurity region in such a manner that said N-type emitter region is located between said first and second P-type base regions and each of said first and second P-type base regions has a portion contacting with said N-type emitter region;

N-type collector regions selectively disposed in a surface of said second P-type base region so as to be spaced from said N-type emitter region, and containing N-type impurities at a relatively higher concentration;

a base-collector common electrode contacting with a portion of said N-type collector region exposed at the same level with an exposed surface of said second P-type

base region, and also contacting partly with said exposed surface of said second P-type base region; and

an anode-emitter common electrode contacting with an exposed surface of said first P-type base region, wherein

said anode-emitter common electrode is connected to said input/output terminal,

said base-collector common electrode is connected to said ground terminal, and

said N-type emitter region corresponds to said emitter of said NPN transistor and also corresponds to said base of said PNP transistor.

11. The semiconductor device according to claim 10, further comprising a high-concentration N-type impurity region contacting with an entire surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate, and containing N-type impurities at a relatively higher concentration, wherein

said high-concentration N-type impurity region is connected to a ground potential.

12. The semiconductor device according to claim 10, further comprising a high-concentration N-type impurity region contacting with a surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate, and containing N-type impurities at a relatively higher concentration, wherein

said high-concentration N-type impurity region is maintained at a floating potential.

13. The semiconductor device according to claim 10, further comprising an insulating layer contacting with a surface of said low-concentration N-type impurity region at a second main surface side of said semiconductor substrate.